In the Abstract:

Please replace the abstract on page 40 with the following:

A dual mode, full density/half density SDRAM includes a refresh controller specifically adapted to refresh memory cells of the SDRAM in the half density mode at a rate that is significantly slower than the rate at which the memory cells are refreshed in the full density mode. In the half density mode, the refresh controller increments a counter at a rate that is half the rate the counter is incremented in the full density mode. A refresh trigger pulse, which initiates the refresh of the memory cells, is generated when the counter has incremented to one of a first counter stage in the full density mode and a counter stage two stages beyond the first counter stage in the half density mode. Circuitry is also provided for ignoring some auto-refresh commands applied to the SDRAM in the half density mode so that the memory cells are also refreshed less frequently in the auto-refresh mode. The SDRAM also includes circuitry for remapping one of the row address bits for use as a column address bit in the half density mode so that the SDRAM can interface with system adapted for conventional dual mode SDRAMs.

## REMARKS

It has come to the Applicants attention that Claim 42 was allowed in the parent file, Application No. 09/803,365, filed March 8, 2001, U.S. Patent No. 6,449,203. To avoid duplicate allowance of Claim 42, Applicants hereby cancel Claim 42 in this instant application. Applicants have also amended the specification and abstract.

Claims 11, 12, 14, 27, 28, 36 and 37 are now in proper form. Applicants respectfully request a Supplemental Notice of Allowance reflecting the changes made.